ABSTRACT

A system interface having: a plurality of front end directors adapted for coupling to a host computer/server; a plurality of back end directors adapted for coupling to a bank of disk drives; a data transfer section having cache memory; a cache memory manager; and, a message network. The cache memory is coupled to the plurality of front end and back end directors. The messaging network operates independently of the data transfer section and is coupled to the plurality of front end and back end. The front end and back end directors control data transfer between the host computer/server and the bank of disk drives in response to messages passing between the front end directors and the back end directors through the messaging network to facilitate data transfer between host computer/server and the bank of disk drives. The data passes through the cache memory in the data transfer section as such data passes between the host computer and the bank of disk drives. The system includes a cache memory manager having therein a memory for storing a map maintaining a relationship between data stored in the cache memory and data stored in the disk drives. The cache memory manager provides an interface between the host computer, the bank of disk drives and the cache memory for determining for the directors whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory. With such an arrangement, the cache memory in the data transfer section is not burdened with the task of transferring the director messaging but rather a messaging network is provided, operative independent of the data transfer section, for such messaging thereby increasing the operating bandwidth of the system interface. Further, the cache memory is no longer burdened with the task of evaluating whether data to be read from the disk drives, or data to be written to the disk drives, resides in the cache memory. The cache memory manager, plurality of front end directors, plurality of back end directors and cache memory are interconnected through a packet switching network.